## Product Overview

Implementing a USB peripheral typically requires in-depth knowledge of the USB protocol, a considerable firmware and software development effort and rigorous compliance testing. But now there's an alternative.

The QuickUSB™ QUSB2 Plug-In Module makes adding Hi-Speed USB 2.0 to new or existing products quick and easy by integrating all the hardware, firmware and software needed to implement a general-purpose USB device as an easy-to-use plug-in module. The QuickUSB™ Plug-In Module also includes the QuickUSB™ Library.

The QuickUSB plug-in module contains hardware parallel and serial ports that circuit designer connects to circuitry in the peripheral. The QuickUSB library provides user-callable software functions that transfer data to and from the hardware ports over the USB. So the designer gets multiple ports of flexible, high-speed USB connectivity and no detailed knowledge of USB is required.

## Functional Block Diagram

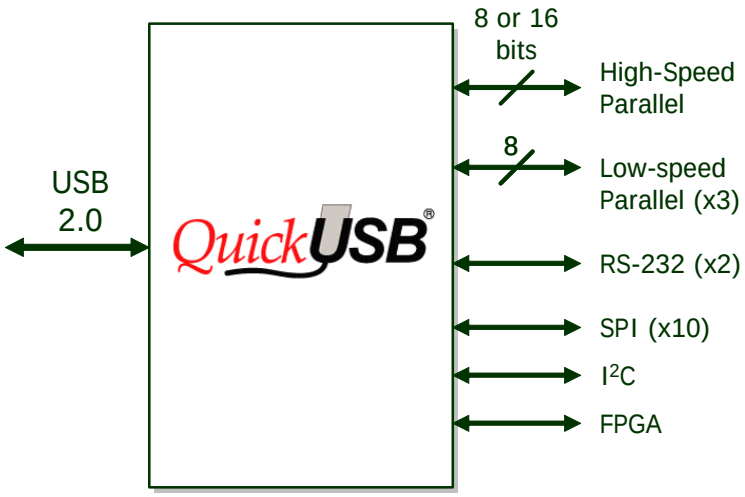


*Figure 1 – QUSB2 Functional Block Diagram*

## Functional Description

## The QuickUSB Plug-In Module

The QuickUSB QUSB2 Plug-In Module is a 2" x 1 ½" circuit board that implements a bus-powered Hi-speed USB 2.0 endpoint terminating in a single 80-pin target interface connector. The mating connector is a Hirose FX8-80S_SV.

The target interface consists of:

- One 8 or 16-bit High-Speed Parallel Port (HSPP)
- Up to five general-purpose 8-bit parallel I/O ports
- Two RS-232 compatible ports
- One I²C master port
- One soft SPI master port supporting up to 10 slave devices
- One FPGA configuration port (Altera PS or Xilinx SS)

## High-Speed Parallel Port

The high-speed parallel port is configurable as an 8 or 16 bit synchronous parallel port. It delivers a sustained data rate of up to 20 MB/s and a burst rate of up to 96MB/s for packets up to 512 bytes long. The high-speed interface consists of the data port FD[15:0], control lines CMD_DATA, REN, WEN, nREN, nWEN and GPIFADR [8:0]. The port can be used as a multiplexed command/data bus by decoding CMD_DATA (CMD = 0, DATA = 1 in the target logic. Reads are indicated by REN = 1/nREN = 0 and writes are indicated by WEN = 1/nWEN = 0. If the address bus is configured to be active, concurrent with reads or writes the GPIFADR bus contains the address of each data element read from or written to FD [15:0].

## General Purpose Parallel I/O Ports

General purpose I/O pins must be configured to indicate whether they are being used as input or output pins. This is accomplished using library calls documented in the QuickUSB User's Guide.

The parallel ports have multiple functions and may not be available if alternate functions are enabled. The general-purpose I/O ports are ports A, B, C, D & E. Ports B & D are shared with the High-Speed Parallel port. The Port E is shared with FPGA configuration and the soft SPI ports.

## RS-232

The module has two RS-232 ports with a configurable baud rate. Both ports use the same baud rate. These interrupt-driven ports internally buffer data as it arrives and when queried return the contents of the internal buffer.

## $I^2C$

An I2C compatible port is included on the QuickUSB module. The port is a bus master only. The QuickUSB library provides functions to write and read blocks of data to and from I2C peripherals.

## SPI

The module supports SPI peripherals through a 'soft' SPI port, which uses pins on port E. The pins MOSI, SCK, MISO and nSS are shared with the FPGA configuration function and will not interfere with each other *if* the SPI peripherals only drive the MISO when nSS is asserted (nSS=0). By dynamically reallocating port A, the SPI master port can address an additional 8 slave devices.

## FPGA Configuration

The QuickUSB Plug-In module can program Altera or Xilinx programmable logic devices using five pins of port E. When designing your peripheral to use this feature, consult the FPGA manufacturer's documentation'. The QuickUSB module provides the appropriate signals required to configure FPGAs in passive serial/slave serial mode. If more than one device must be configured over the interface, the devices should be 'daisy-chained' and the programming files combined into a single file.

## The QuickUSB Library

The QuickUSB® Library is included with the QUSB2 and provides the programming language interface to the QuickUSB Plug-in Module. The QuickUSB Library abstracts the complexity of USB 2.0 behind a port-based programmer's interface. A complete description of each library function is provided in the QuickUSB™ User's Guide. The QuickUSB Library includes support for many popular programming languages including Visual C, Visual Basic, Delphi, C++ Builder and LabView.

## QuickUSB Module Pin Descriptions

| Pin | Name | Dir | Description | Pin | Name | Dir | Description |
|---|---|---|---|---|---|---|---|
| 1 | GND | N/A | Ground | 2 | +5V | N/A | Unregulated +5V from the USB bus (300mA total) |
| 3 | PA0 | I/O | Port A, Bit 0 / nSS2 | 4 | RESET_B | OD | FX2 reset, Active low. |
| 5 | PA1 | I/O | Port A, Bit 1 / nSS3 | 6 | CLKOUT | Output | 48MHz CPU clock |
| 7 | PA2 | I/O | Port A, Bit 2 / nSS4 | 8 | IFCLK | Output | 48MHz GPIO clock |
| 9 | PA3 | I/O | Port A, Bit 3 / nSS5 | 10 | INT4 | Input | 8051 INT4 IRQ. Active high, edge sensitive |
| 11 | PA4 | I/O | Port A, Bit 4 / nSS6 | 12 | RXD_0 | Input | Serial Port 0 RS-232 RxD |
| 13 | PA5 | I/O | Port A, Bit 5 / nSS7 | 14 | TXD_0 | Output | Serial Port 0 RS-232 TxD |
| 15 | PA6 | I/O | Port A, Bit 6 / nSS8 | 16 | TXD_1 | Output | Serial Port 1 RS-232 TxD |
| 17 | PA7 | I/O | Port A, Bit 7 / nSS9 | 18 | RXD_1 | Input | Serial Port 1 RS-232 RxD |
| 19 | GND | N/A | Ground | 20 | +5V | N/A | Unregulated +5V from the USB bus (300mA total) |
| 21 | PB0 | I/O | Port B, Bit 0 / FD0 | 22 | CTL0 | Output | GPIF ctl out 0 / CMD_DATA |
| 23 | PB1 | I/O | Port B, Bit 1 / FD1 | 24 | CTL1 | Output | GPIF ctl out 1 / REN |
| 25 | PB2 | I/O | Port B, Bit 2 / FD2 | 26 | CTL2 | Output | GPIF ctl out 2 / WEN |
| 27 | PB3 | I/O | Port B, Bit 3 / FD3 | 28 | CTL3 | Output | GPIF ctl out 3 / nREN |
| 29 | PB4 | I/O | Port B, Bit 4 / FD4 | 30 | CTL4 | Output | GPIF ctl out 4 / nWEN |
| 31 | PB5 | I/O | Port B, Bit 5 / FD5 | 32 | CTL5 | Output | GPIF ctl out 5 / AEN |
| 33 | PB6 | I/O | Port B, Bit 6 / FD6 | 34 | RXD0 | Input | Serial Port 0 TTL RxD (Do not use if U1 is populated) |
| 35 | PB7 | I/O | Port B, Bit 7 / FD7 | 36 | TXD0 | Output | Serial Port 0 TTL RxD (Do not use if U1 is populated) |
| 37 | GND | N/A | Ground | 38 | +5V | N/A | Unregulated +5V from the USB bus (300mA total) |
| 39 | PC0 | I/O | Port C, Bit 0 / GPIFADR0 | 40 | RDY0 | Input | GPIF input signal 0 |
| 41 | PC1 | I/O | Port C, Bit 1 / GPIFADR1 | 42 | RDY1 | Input | GPIF input signal 1 |
| 43 | PC2 | I/O | Port C, Bit 2 / GPIFADR2 | 44 | RDY2 | Input | GPIF input signal 2 |
| 45 | PC3 | I/O | Port C, Bit 3 / GPIFADR3 | 46 | RDY3 | Input | GPIF input signal 3 |
| 47 | PC4 | I/O | Port C, Bit 4 / GPIFADR4 | 48 | RDY4 | Input | GPIF input signal 4 |
| 49 | PC5 | I/O | Port C, Bit 5 / GPIFADR5 | 50 | RDY5 | Input | GPIF input signal 5 |
| 51 | PC6 | I/O | Port C, Bit 6 / GPIFADR6 | 52 | RXD1 | Input | Serial Port 1 TTL RxD (Do not use if U1 is populated) |
| 53 | PC7 | I/O | Port C, Bit 7 / GPIFADR7 | 54 | TXD1 | Output | Serial Port 1 TTL RxD (Do not use if U1 is populated) |
| 55 | GND | N/A | Ground | 56 | +5V | N/A | Unregulated +5V from the USB bus (300mA total) |
| 57 | PD0 | I/O | Port D, Bit 0 / FD8 | 58 | PE0 | I/O | Port E, Bit 0 / DATA0 / MOSI |
| 59 | PD1 | I/O | Port D, Bit 1 / FD9 | 60 | PE1 | I/O | Port E, Bit 1 / DCLK / SCK |
| 61 | PD2 | I/O | Port D, Bit 2 / FD10 | 62 | PE2 | I/O | Port E, Bit 2 / nCE |
| 63 | PD3 | I/O | Port D, Bit 3 / FD11 | 64 | PE3 | I/O | Port E, Bit 3 / nCONFIG |
| 65 | PD4 | I/O | Port D, Bit 4 / FD12 | 66 | PE4 | I/O | Port E, Bit 4 / nSTATUS |
| 67 | PD5 | I/O | Port D, Bit 5 / FD13 | 68 | PE5 | I/O | Port E, Bit 5 / CONF_DONE / MISO (see note) |
| 69 | PD6 | I/O | Port D, Bit 6 / FD14 | 70 | PE6 | I/O | Port E, Bit 6 / nSS0 |
| 71 | PD7 | I/O | Port D, Bit 7 / FD15 | 72 | PE7 | I/O | Port E, Bit 7 / GPIFADR8 / nSS1 |
| 73 | SCL | OD | Clock for I2C interface | 74 | WAKEUP_B | Input | USB Wakeup. Active low. |
| 75 | SDA | OD | Data for I2C interface | 76 | SW_PG | Output | Power good signal, Active high when +5V is good. |
| 77 | T0 | Input | Input for Timer0 | 78 | T1 | Input | Input for Timer1 |
| 79 | GND | N/A | Ground | 80 | +5V | N/A | +5V |

*Table 1 – QUSB2 Pin Description*

## QuickUSB Socket Mechanical Drawing

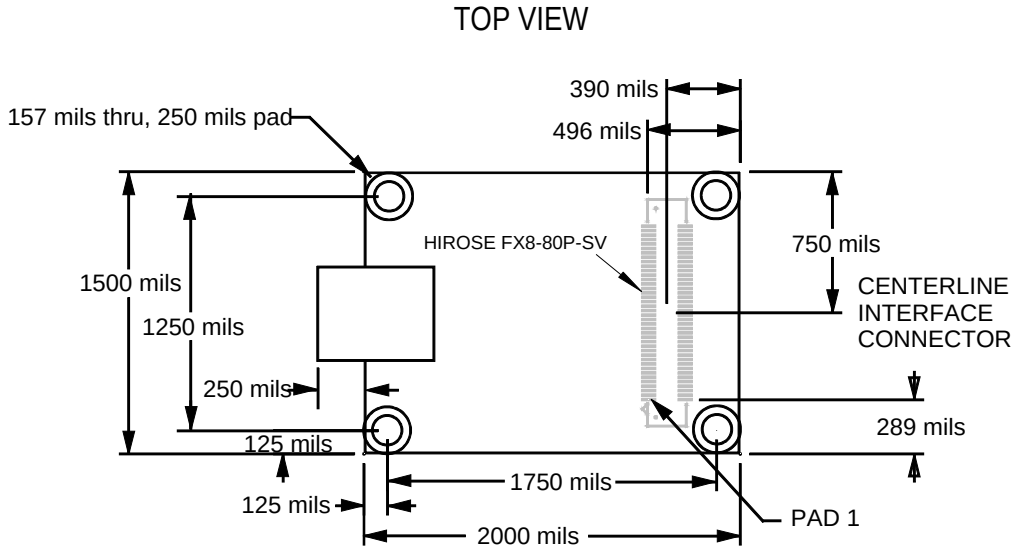


*Figure 2- QuickUSB Socket Layout*

## Contact

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